

MC74VHC1GT50

Noninverting Buffer / CMOS Logic Level Shifter

TTL-Compatible Inputs

The MC74VHC1GT50 is a single gate noninverting buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The device input is compatible with TTL-type input thresholds and the output has a full 5 V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic-level translator from 3 V CMOS logic to 5 V CMOS Logic or from 1.8 V CMOS logic to 3 V CMOS Logic while operating at the high-voltage power supply.

The MC74VHC1GT50 input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows the MC74VHC1GT50 to be used to interface high voltage to low voltage circuits. The output structures also provide protection when $V_{CC} = 0$ V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

Features

- Designed for 1.65 V to 5.5 V_{CC} Operation
- High Speed: $t_{PD} = 3.5$ ns (Typ) at $V_{CC} = 5$ V
- Low Power Dissipation: $I_{CC} = 1$ μ A (Max) at $T_A = 25^\circ$ C
- TTL-Compatible Inputs: $V_{IL} = 0.8$ V; $V_{IH} = 2.0$ V, $V_{CC} = 5$ V
- CMOS-Compatible Outputs: $V_{OH} > 0.8 V_{CC}$; $V_{OL} < 0.1 V_{CC}$ @Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: FETs = 104; Equivalent Gates = 26
- Pb-Free Packages are Available

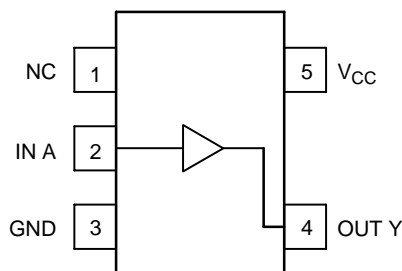


Figure 1. Pinout (Top View)

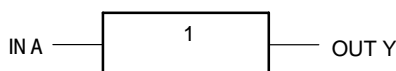


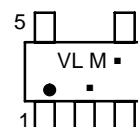
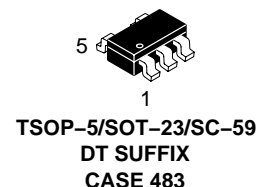
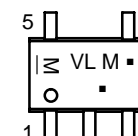
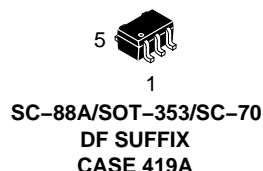
Figure 2. Logic Symbol



ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAMS



VL = Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

PIN ASSIGNMENT

1	NC
2	IN A
3	GND
4	OUT Y
5	V_{CC}

FUNCTION TABLE

A Input	Y Output
L	L
H	H

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MC74VHC1GT50

MAXIMUM RATINGS

Symbol	Characteristics	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
V _{IN}	DC Input Voltage	-0.5 to +7.0	V
V _{OUT}	DC Output Voltage	V _{CC} = 0 High or Low State -0.5 to 7.0 -0.5 to V _{CC} + 0.5	V
I _{IK}	Input Diode Current	-20	mA
I _{OK}	Output Diode Current	V _{OUT} < GND; V _{OUT} > V _{CC}	mA
I _{OUT}	DC Output Current, per Pin	+25	mA
I _{CC}	DC Supply Current, V _{CC} and GND	+50	mA
P _D	Power dissipation in still air	SC-88A, TSOP-5 200	mW
θ _{JA}	Thermal resistance	SC-88A, TSOP-5 333	°C/W
T _L	Lead temperature, 1 mm from case for 10 secs	260	°C
T _J	Junction temperature under bias	+150	°C
T _{stg}	Storage temperature	-65 to +150	°C
V _{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3) > 2000 > 200 N/A	V
I _{Latchup}	Latchup Performance	Above V _{CC} and Below GND at 125°C (Note 4)	±500 mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Tested to EIA/JESD22-A114-A
2. Tested to EIA/JESD22-A115-A
3. Tested to JESD22-C101-A
4. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
V _{CC}	DC Supply Voltage	1.65	5.5	V
V _{IN}	DC Input Voltage	0.0	5.5	V
V _{OUT}	DC Output Voltage	V _{CC} = 0 High or Low State 0.0 0.0	5.5 V _{CC}	V
T _A	Operating Temperature Range	-55	+125	°C
t _r , t _f	Input Rise and Fall Time	V _{CC} = 3.3 V ± 0.3 V V _{CC} = 5.0 V ± 0.5 V	0 100 20	ns/V

Device Junction Temperature versus Time to 0.1% Bond Failures

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

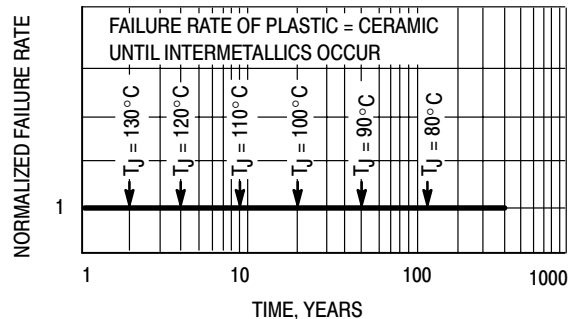


Figure 3. Failure Rate vs. Time Junction Temperature

MC74VHC1GT50

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} (V)	T _A = 25°C			T _A ≤ 85°C		-55 ≤ T _A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	Minimum High-Level Input Voltage		1.65 to 2.29	0.50 V _{CC}			0.50 V _{CC}		0.50 V _{CC}		V
			2.3 to 2.99	0.45 V _{CC}			0.45 V _{CC}		0.45 V _{CC}		
			3.0	1.4			1.4		1.4		
			4.5	2.0			2.0		2.0		
V _{IL}	Maximum Low-Level Input Voltage		1.65 to 2.29			0.10 V _{CC}		0.10 V _{CC}		0.10 V _{CC}	V
			2.3 to 2.99			0.15 V _{CC}		0.15 V _{CC}		0.15 V _{CC}	
			3.0			0.53		0.53		0.53	
			4.5			0.8		0.8		0.8	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} = V _{IH} I _{OH} = -50 μA	1.65 to 2.99	V _{CC} - 0.1			V _{CC} - 0.1		V _{CC} - 0.1		V
			3.0	2.9	3.0		2.9		2.9		
		4.5	4.4	4.5		4.4		4.4		4.4	
		V _{IN} = V _{IH} I _{OH} = -4 mA I _{OH} = -8 mA	3.0	2.58			2.48		2.34		V
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} = V _{IL} I _{OL} = 50 μA	1.65 to 2.99		0.0	0.1		0.1		0.1	V
			3.0		0.0	0.1		0.1		0.1	
		4.5			0.1		0.1		0.1		
		V _{IN} = V _{IL} I _{OL} = 4 mA I _{OL} = 8 mA	3.0			0.36		0.44		0.52	V
4.5			0.36		0.44		0.52	0.52			
I _{IN}	Maximum Input Leakage Current	V _{IN} = 5.5 V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			1.0		20		40	μA
I _{CC(T)}	Quiescent Supply Current	Input: V _{IN} = 3.4 V	5.5			1.35		1.50		1.65	mA
I _{OPD}	Output Leakage Current	V _{OUT} = 5.5 V	0.0			0.5		5.0		10	μA

AC ELECTRICAL CHARACTERISTICS C_{load} = 50 pF, Input t_r = t_f = 3.0 ns

Symbol	Parameter	Test Conditions	T _A = 25°C			T _A ≤ 85°C		-55 ≤ T _A ≤ 125°C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A to Y	V _{CC} = 1.8 ± 0.15 V C _L = 15 pF			16.6		18.0		22.0	ns
		V _{CC} = 2.5 ± 0.2 V C _L = 15 pF			13.3		14.5		17.5	ns
		V _{CC} = 2.5 ± 0.2 V C _L = 50 pF			19.5		22.0		25.5	ns
		V _{CC} = 3.3 ± 0.3 V C _L = 15 pF		4.5	10.0		11.0		13.0	ns
C _{IN}	Maximum Input Capacitance	V _{CC} = 3.3 ± 0.3 V C _L = 50 pF		6.3	13.5		15.0		17.5	ns
		V _{CC} = 5.0 ± 0.5 V C _L = 15 pF		3.5	6.7		7.5		8.5	ns
C _{IN}	Maximum Input Capacitance	V _{CC} = 5.0 ± 0.5 V C _L = 50 pF		4.3	7.7		8.5		9.5	ns
				5	10		10		10	pF

		Typical @ 25°C, V _{CC} = 5.0 V	
C _{PD}	Power Dissipation Capacitance (Note 5)	12	
		pF	

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

MC74VHC1GT50

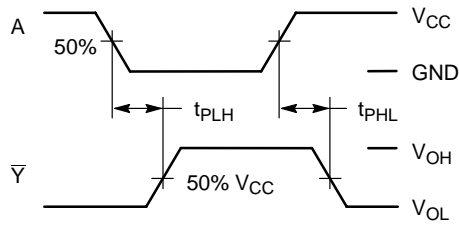
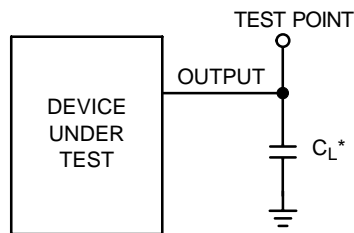


Figure 4. Switching Waveforms



*Includes all probe and jig capacitance

Figure 5. Test Circuit

ORDERING INFORMATION

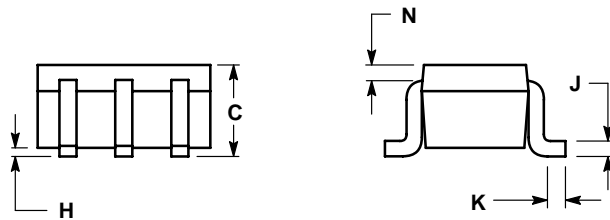
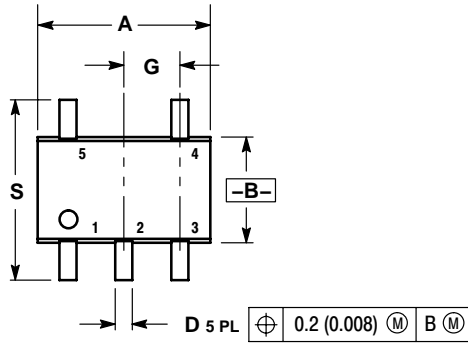
Device	Package	Shipping†
MC74VHC1GT50DFT1	SC-88A / SOT-353 / SC-70	3000 / Tape & Reel
M74VHC1GT50DFT1G	SC-88A / SOT-353 / SC-70 (Pb-Free)	
MC74VHC1GT50DFT2	SC-88A / SOT-353 / SC-70	
M74VHC1GT50DFT2G	SC-88A / SOT-353 / SC-70 (Pb-Free)	
MC74VHC1GT50DTT1	TSOP-5 / SOT-23 / SC-59	
M74VHC1GT50DTT1G	TSOP-5 / SOT-23 / SC-59 (Pb-Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MC74VHC1GT50

PACKAGE DIMENSIONS

SC-88A, SOT-353, SC-70
CASE 419A-02
ISSUE J

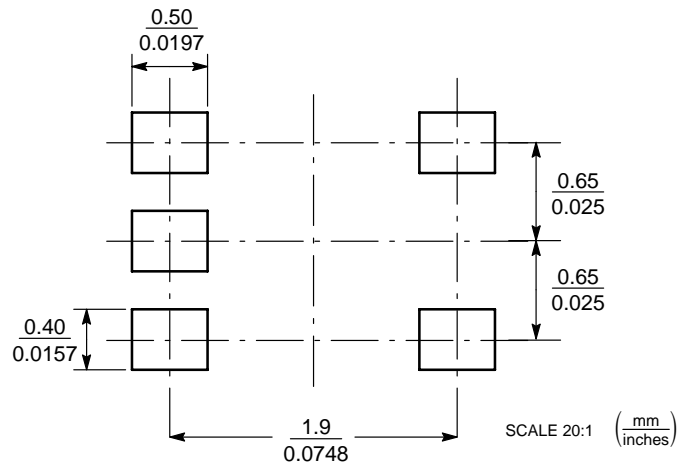


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

SOLDERING FOOTPRINT*

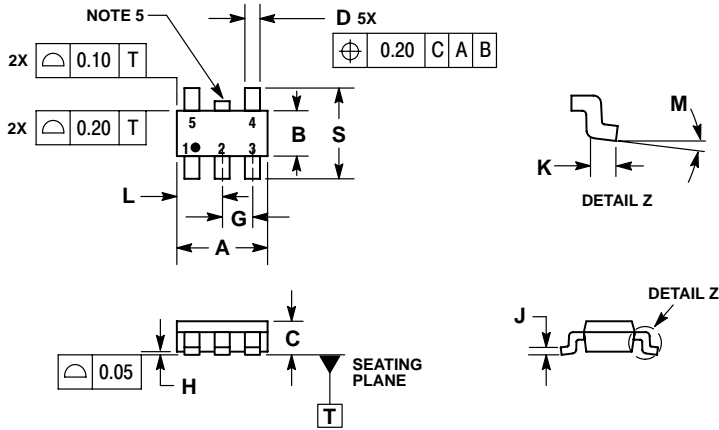


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74VHC1GT50

PACKAGE DIMENSIONS

TSOP-5
CASE 483-02
ISSUE G

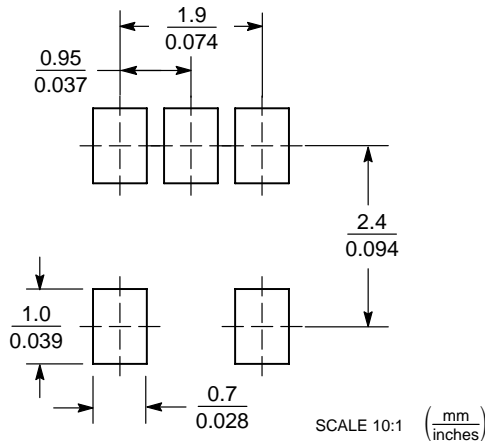


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

DIM	MILLIMETERS	
	MIN	MAX
A	3.00 BSC	
B	1.50 BSC	
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
L	1.25	1.55
M	0°	10°
S	2.50	3.00

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative